Swiss Federal Institute of Technology Zurich
Signal and Information Processing Laboratory

Analog Reed Miller Decoder Tester RMT04

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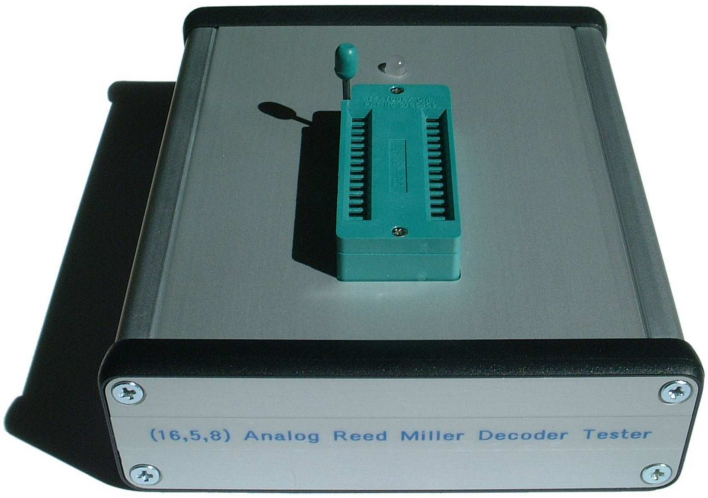


Contents

1 Overview

The RMT04 is aimed to test the (16,5,8) Analog Reed Miller Decoder Chip designed at ISI by HAL/MUF/PPM in May 2004.

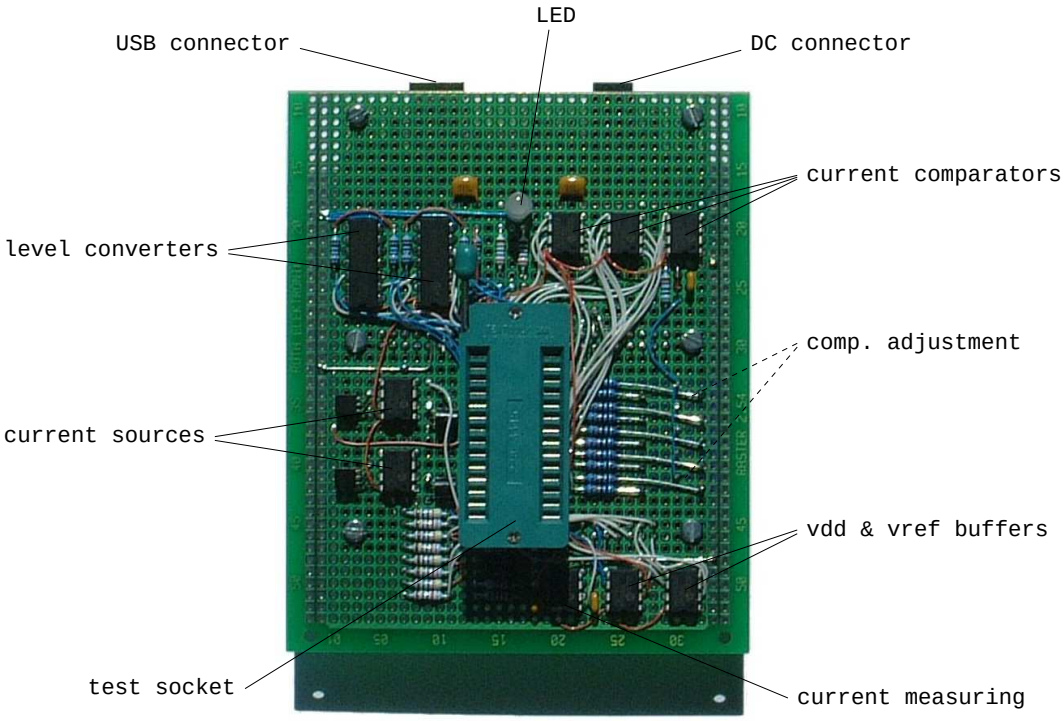


Figure 1: Driver Board with Test Socket

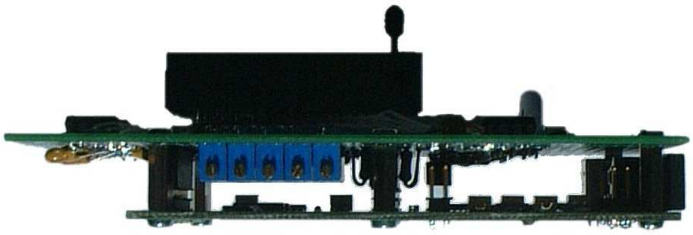


Figure 2: Driver Board piggyback on FX2 USB Board

2 FX2 USB Board

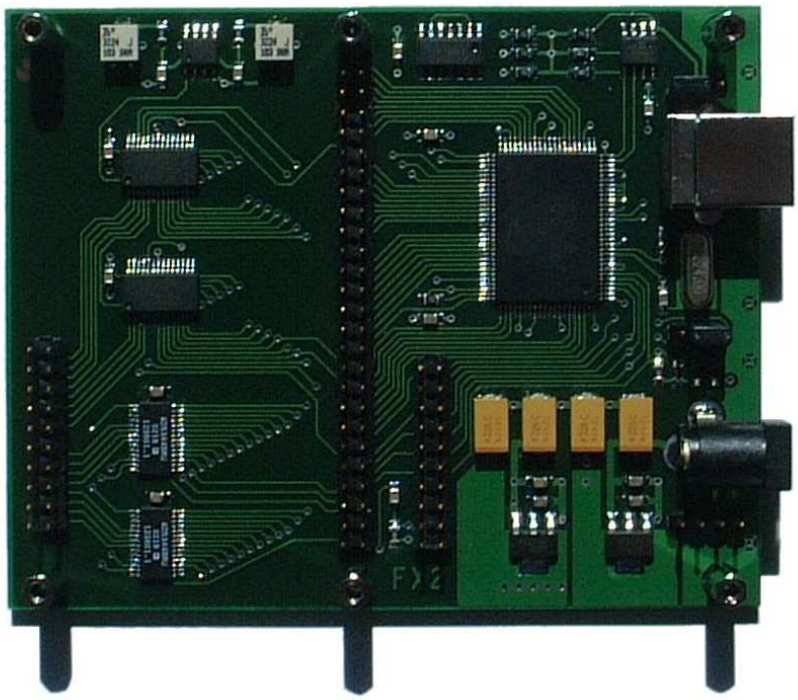


Figure 3: FX2 Board with USB Controller and DACs/ADCs

2.1 Controller

The USB 2.0 interface is built up on a four layer PCB. The central part is a Cypress CY7C68013 controller (aka FX2). This chip integrates an USB2.0 transceiver, an enhanced 8051 microcontroller and a fast parallel peripheral interface. Program code can be uploaded from the USB or the chip can boot from a serial EEPROM. See [1], [2], [3], [4] and application notes from Cypress to learn more about this powerful controller.

2.2 Analog I/O

The FX2 board features two ADS7842 Four Channel 12Bit ADCs and two AD5344 Four Channel 12Bit DACs. The sampling rate is somewhat above 100kHz at the given supply voltage of 3.3V. Reference voltages are adjustable for a full scale value of 0.1 to 3.3V for analog inputs and 0.25 to 3.3V for analog outputs. For the RMT04 both reference voltages are set to 2.048V.

2.3 Power Supply

The tester can be fully bus powered from the USB. The FX2 enumerates for a current consumption of 100mA but when running at high speed USB transfer rates, the power device will draw up to 150mA.

A DC connector is provided for an external 7 Volt power supply if you can't accept the relatively high power consumption from USB. There is a jumper on the FX2 board that must be changed for external power.

The CY7C68013 controller runs from a regulated 3.3V power supply realized on the FX2 board. The same power supply is also used for the driver board of the tester.

Figure 4: Rear View with DC Input and USB Connector

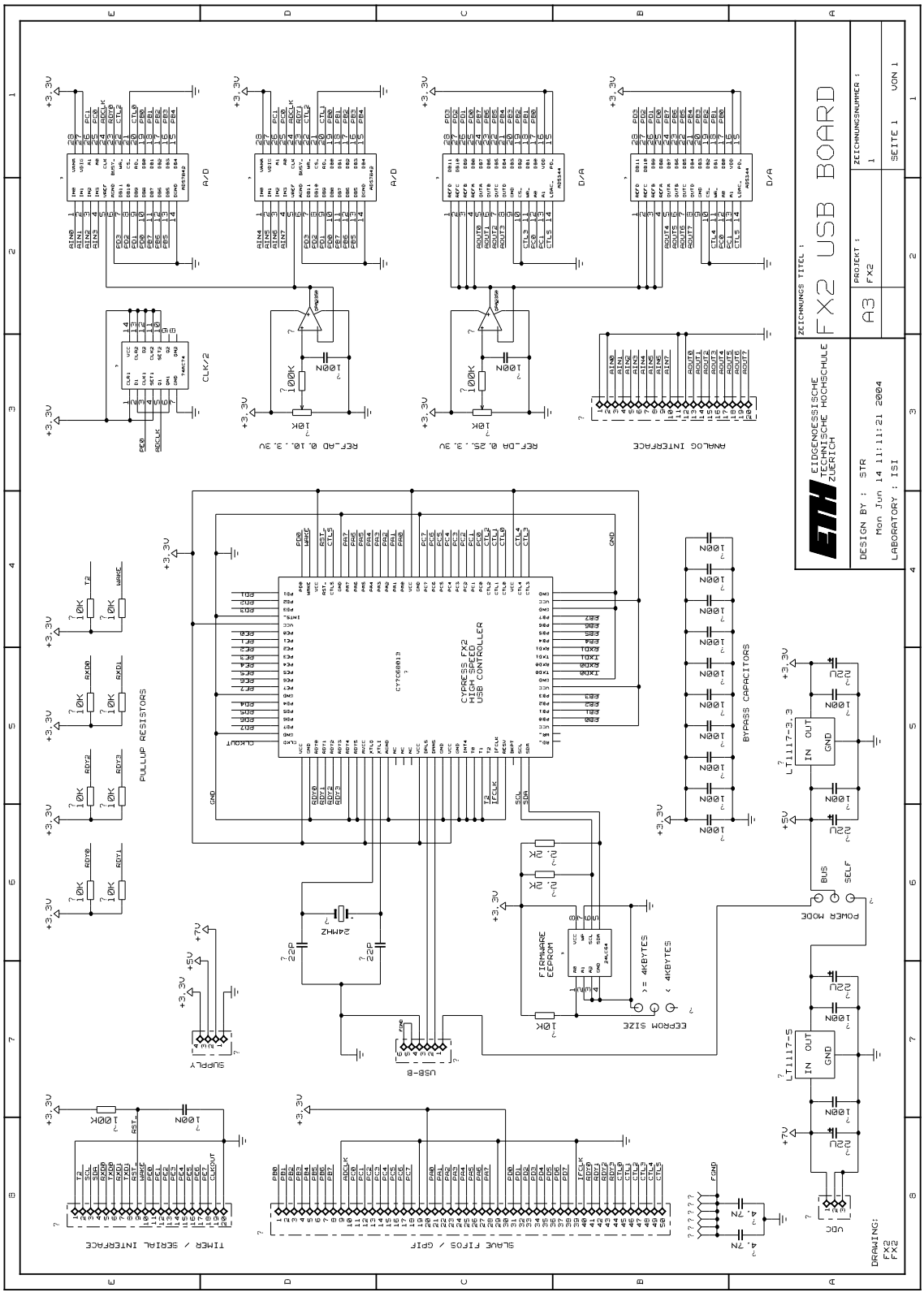


Figure 5: FX2 Board Schematic

3 Driver Board

3.1 Generation of Voltages and Currents

All eight DAC Outputs from the FX2 board are used: three of them are buffered with op-amps to provide the voltage sources VDD, REFA, REFB and one is connected over a 1MΩ resistor to BIAS. The remaining four DAC channels are used to control the current sources (see Figure 6).

The DAC reference voltage (2.048V) is routed to AIN7 through a 10kΩ resistor on the FX2 board to make it available for the current sources. On the driver board the reference voltage is slightly reduced with a 1MΩ resistor to ground and then buffered with a 100n capacitor and an op-amp. Since `Vref` for the current source is reduced to 2.028V but the range of `Vin` still goes up to 2.048V, offset errors can be easily corrected by software.

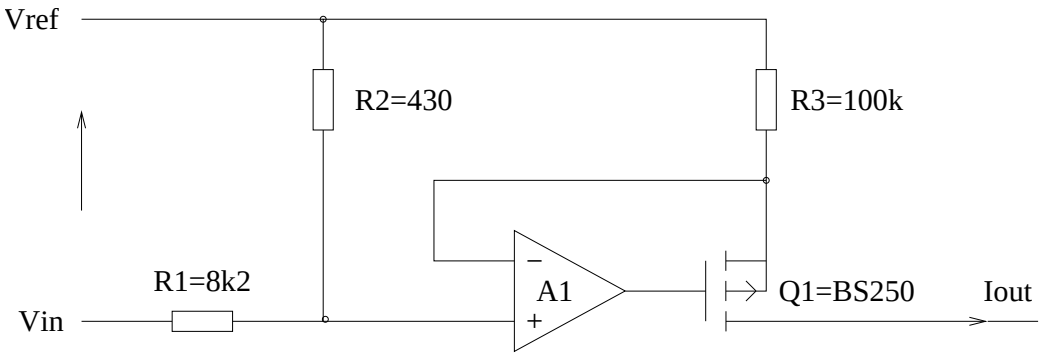


Figure 6: Current Source

3.2 Measuring of Test Currents

To observe the hold characteristics of the input circuit the two test outputs (`TEST<0>` and `TEST<1>`) can be measured simultaneously. The simple current to voltage conversion circuitry shown in Figure 7 directly measures the voltage that shows up on a grounded shunt resistor.

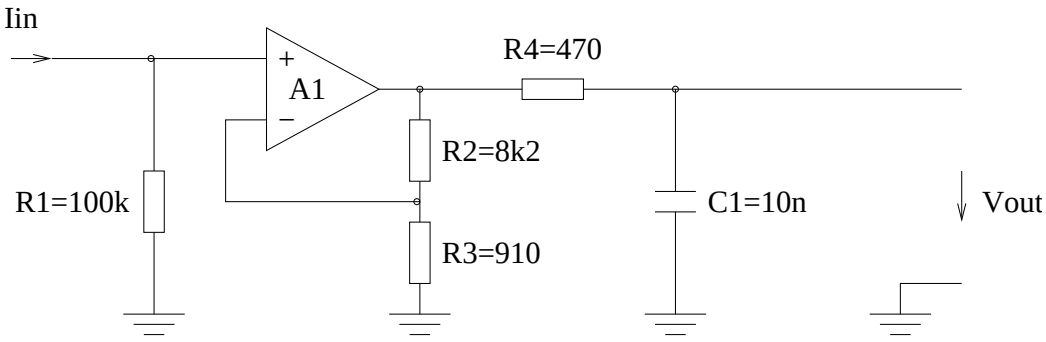


Figure 7: Current to Voltage Translation

3.3 Digital Outputs

Five output ports control the decoder's digital inputs. Since the FX2 controller has 3.3V level for digital I/Os and the tested chip runs at 1.8V a level translation is needed. Figure 8 shows the interface used to drive the lower voltage digital inputs of the decoder chip. The open collector outputs of a 74HC266 are pulled up with 10kΩ resistors to VDD of the test socket (XNOR gates allow easy changing from positive to negative logic). The pullups (`R2`) for `CLK` and `CSW` are reduced to 2.5kΩ to achieve a faster rising edge.

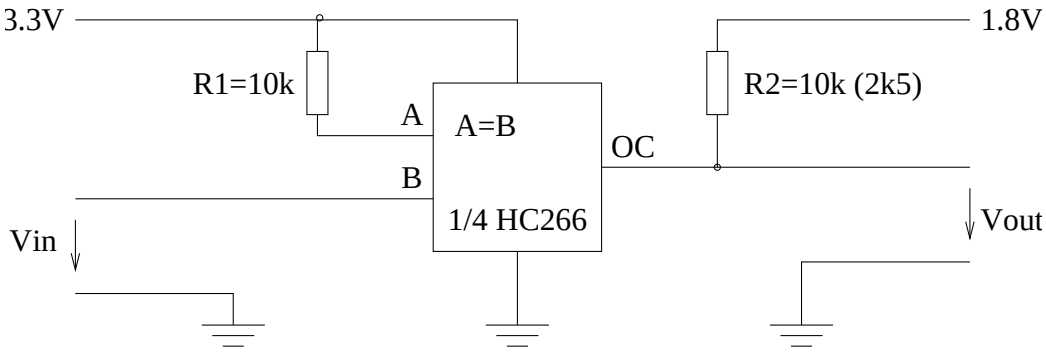


Figure 8: Level Translator

3.4 Digital Inputs

Five digital input ports on the FX2 board are used to read the decoder result. The output of the decoder are five current output pairs. A comparator as shown in Figure 9 is assigned to each pair of currents to make a decision whether the resulting bit is 0 or 1. For a good accuracy the the comparator should be balanced with P5.

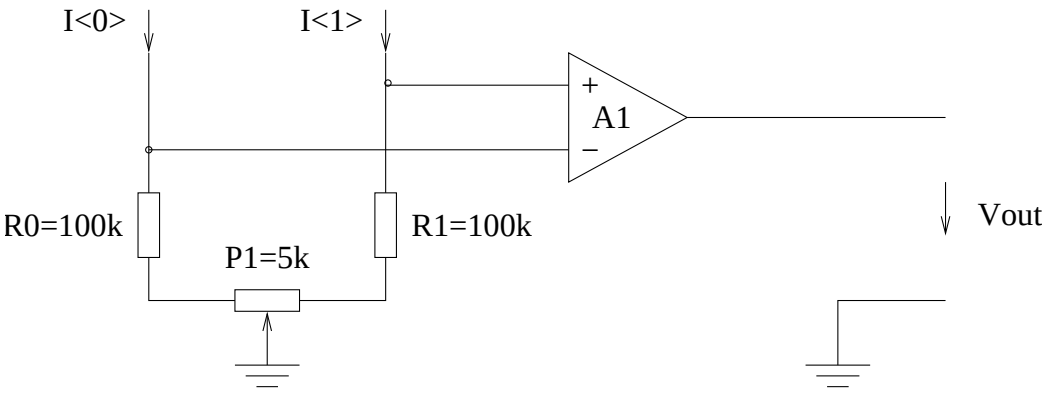


Figure 9: Current Comparator

3.5 Calibration

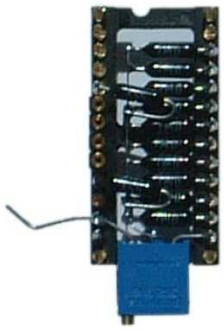


Figure 10: Dummy Device used for Calibration

Figure 10 shows a calibration dummy to be inserted in the test socket. A pair of precision resistors (1MΩ, 0.1%, manually selected for good matching) is asigned to each current comparator. With a potentiometer the sum current can be adjusted.

To calibrate the current comparators, run a program that repeatedly reads and reports the comparator outputs (PA4..PA0). Then adjust the the five blue potentimeters on the bottom side of the driver board.

Four sockets `In<0..3>` facilitate current measuring when evaluating software calibration values for the current sources.

A short piece of wire on a GND pin is convenient to attach an oscilloscope probe when checking the timing of test cycles.

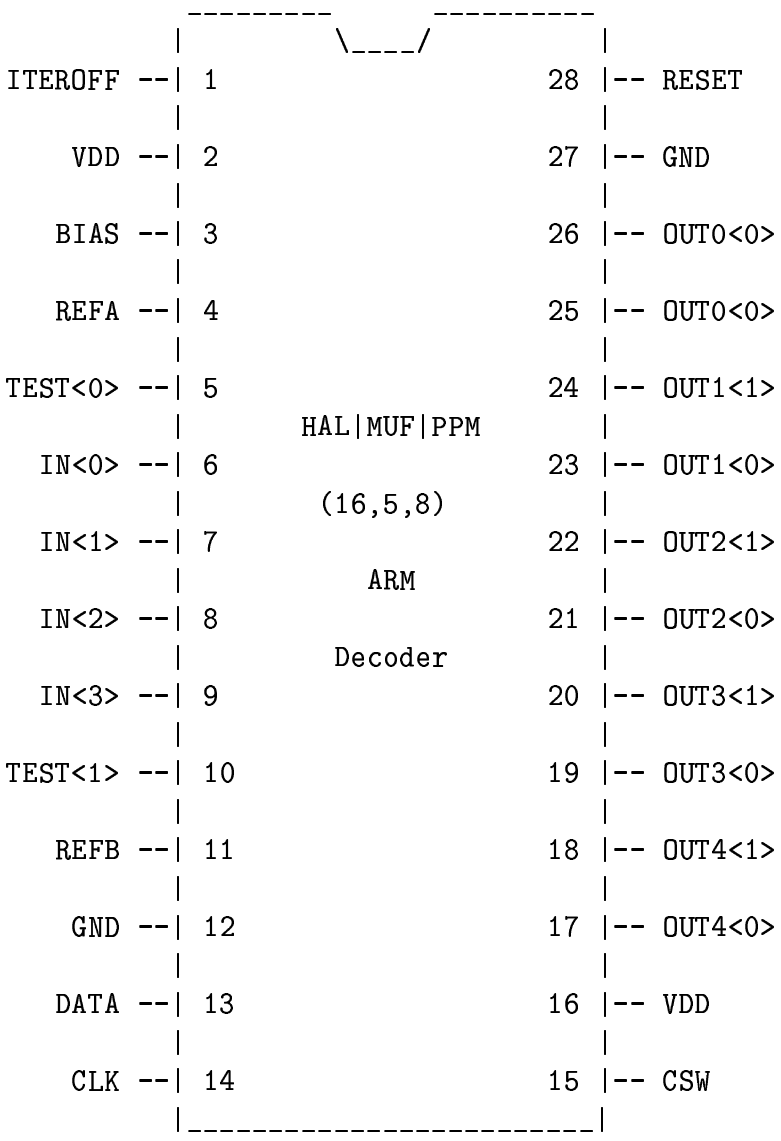
3.6 Pin Assignment on FX2 Board

GPIF Connector			
name	pin number	dir	purpose
GND	9, 19, 29, 39	–	Ground
VDD	20, 30	–	3.3V Power Supply
PA0	21	in	`OUT<0>` decoder result bit
PA1	22	in	`OUT<1>` decoder result bit
PA2	23	in	`OUT<2>` decoder result bit
PA3	24	in	`OUT<3>` decoder result bit
PA4	25	in	`OUT<4>` decoder result bit
PA6	27	out	`ITEROFF` decoder mode
PA7	28	out	`RESET` soft gates reset
PC2	13	out	`DATA` shift register data
PC3	14	out	`CLK` shift register clock
PC4	15	out	`CSW` capacitor switch
PC6	17	out	red led on when low
PC7	18	out	green led on when low

Analog Interface			
name	pin number	dir	purpose
GND	1, 2, 11, 12	–	`GND`
AIN0	3	in	`TEST<0>` current measuring
AIN4	7	in	`TEST<1>` current measuring
AIN7	10	out	Vref (2.048V, 10kΩ)
AOUT0	13	out	`In<0>` current source
AOUT1	14	out	`In<1>` current source
AOUT2	15	out	`In<2>` current source
AOUT3	16	out	`In<3>` current source
AOUT4	17	out	`VDD` supply voltage
AOUT5	18	out	`REFA` supply voltage
AOUT6	19	out	`REFB` supply voltage
AOUT7	20	out	`BIAS` control

4 The (16,5,8) ARM Decoder

4.1 Pinout



The chip is fabricated in an IBM 0.18μm CMOS process and mounted in a 0.3 Inches wide 28pin CERDIP.

4.2 Pin Description

GND	Connect both GND pins to ground level.
VDD	Both VDD pins must be connected to the 1.8V supply.
REFA	Provide a voltage source of 0.45V for REFA.
REFB	Provide a voltage source of 1.35V for REFB.
BIAS	Bias sets the working current for the analog decoder. Feed a current of 1μA to this input.
IN<0..3>	The four current inputs are used to set the 32 decoder input currents in eight steps.
OUT<0..4>	These five pairs of output currents show the result of the decoding process.
TEST<0..1>	Two current outputs to observe the behaviour of the current input holding circuit.
DATA	A 9 bit shift register is used to select a block of four input currents. The ninth block is not connected to the decoder but to a test block from which two currents are mirrored to pins TEST<0..1>. Clear the shift register first by clocking in nine low bits from the DATA pin; then shift in a single high bit that selects the input block.
CLK	The shift register is loaded from DATA at the rising edge of CLK.
CSW	Capswitch connects the input holding capacitors of the selected input block to the input stage.
RESET	When RESET is released decoding is started.
ITEROFF	The iterating mode of the decoder can be turned off with this input.

4.3 Decoder Timing

Due to the limited pin count of the ARM chip the array of input currents must be serially loaded. Two current pairs are loaded in a step so eight steps are needed to apply all 16 input current pairs. A ninth step loads a test circuit that was built in to verify the functionality of current sample and hold stages. A shift register is used to address the nine stages. The state of this shift register is undefined at power up and the user must take care that only a single flipflop is active. Figure 11 shows the required timing to load the input word to the decoder.

The rising edge of `CLK` loads `DATA` to the first flipflop of the nine bit FIFO. The active bit is then shifted to the next stage after 80μs. During the 40μs active period of `CSW` (capswitch) the four input currents `IN<0..3>` have to be stable.

When `RESET` is released the decoding process starts. After an adequate settling time the five bit result is sampled by the tester and sent to the host for further examination.

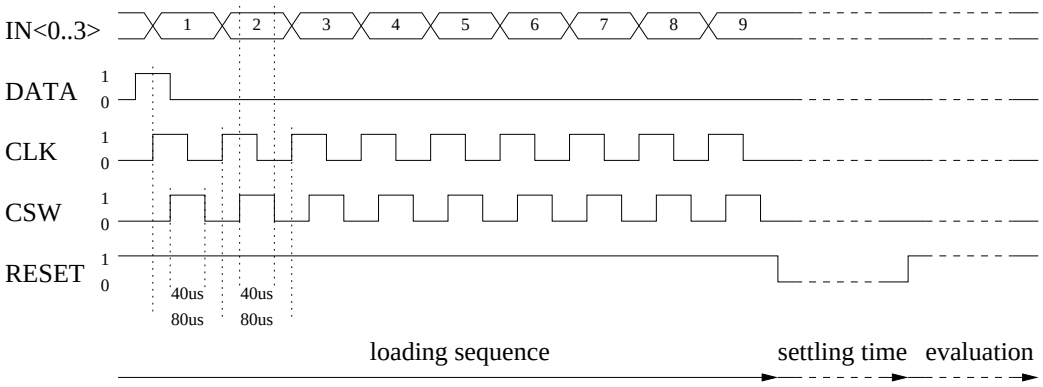


Figure 11: Timing of a Decoding Cycle

5 Software

5.1 Hostprograms

Test programs are written in C using the GNU compiler on a Linux workstation. The main reason for using this platform is the availabilty of libusb (version 0.1.8) that allows userspace applications access to USB devices.

First some utilities have been written to start gathering some experience with libusb and the FX2 chip:

`fxlod` A little utility that allows uploading and running firmware code in Intel hex format to the FX2 controller.

`fxlgen` Loader generator that translates an firmware code file to C code. When this C code is included do a host program it is no more necessary to upload the firmware previously with `fxlod`.

`fxcom` This host program transfers USB bulk in and out packets and reports the achieved data rate.

5.2 Firmware Development with SDCC

The freeware compiler SDCC features good support for 8051 derivates. It is much more comfortable to write the firmware in C than in assembly language. If the performance is important SDCC can handle inline assembler code. Shortly SDCC 2.4.0 has been released but there showed up some problems so I adhered to SDCC 2.3.0. Code examples:

`fxblink` Very simple firmware program that blinks a led; used to verify the function of `fxlod`.

`fxware` Firmware needed to run on the FX2 chip to support *fxcom*.

5.3 GPIF Designer

The General Programmable Interface GPIF supports fast parallel I/O where the FX2 can either be a master or a slave. To set up the core programmable state machine Cypress provides the GPIF Designer, a utility for MS Windows. To create code for the GPIF waveform memories this tool has been used.

References

[1] Cypress, *CY7C68013, High Speed USB Peripheral Controller* (52p)

[2] Cypress, *EZ-USB FX2 Technical Reference Manual* (462p)

[3] Cypress, *EZ-USB FX2 GPIF Primer* (72p)

[4] Cypress, *Introduction to the EZ-USB FX2 GPIF Engine* (13p)

[5] J. K. Rowling, *Harry Potter and the Order of the Phoenix* (768p)

[6] Burr-Brown (Texas Instruments), *ADS7842 12-Bit 4-Channel Parallel Output Sampling Analog to Digital Converter* (16p)

[7] Analog Devices, *AD5344, 2.5V to 5.5V, 500μA, Parallel Interface Quad Voltage-Output 8-/10-/12-Bit DACs* (20p)

[8] Microchip, *MCP6021/2/3/4, Rail-to-Rail I/O 10MHz Op Amps* (28p)

[9] Microchip, *24AA64/24LC64 64K I2C Serial EEPROM* (26p)

[10] Compaq, Hewlett-Packard, Intel, Lucent, Micro$oft, NEC, Philips, *Universal Serial Bus Specification, Revision 2.0* (650p)

[11] http://www.linux-usb.org/usb.ids, *USB Device/Vendor IDs* (123KB)