Swiss Federal Institute of Technology Zurich
Signal and Information Processing Laboratory

Analog (8,4,4) Hamming Decoder Demo Box

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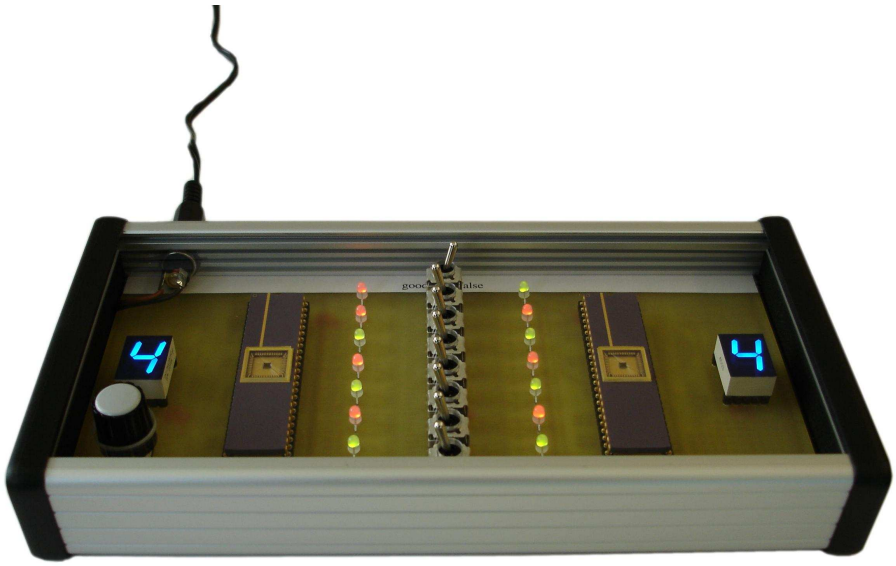

Contents

1 Overview

This small box (206 x 106 x 34mm) demonstrates the function of an (8,4,4) Hamming code. Two analog decoder chips of the same type are used – one for encoding the four bits input data to an 8 bit Hamming code and the other for decoding the code to estimate the original data.

On the communication channel a number of code bits can be inverted. The receiver is able to correct a single bit error.

Since the decoder analyzes the analog state of the received code, input bits can not only be correct or false, but any value in between is also possible. Bits on the demonstration box channel can be turned off to feed a neutral bit state (p0=0.5; p1=0.5) to the receiver: four bits can be turned off without loosing data, provided the four remaining bits are completely correct.

2 Power Supply

A regulated power supply of 6VDC / 0.5A is needed by the demo box. The supply voltage is reduced by an internal LDO regulator to 5V. Though the regulator can accept higher voltages it is not adviseable to feed in voltages abobe 7V because termal loss could be too high.

Figure 1: Power connector: center pin is positive

3 Encoder

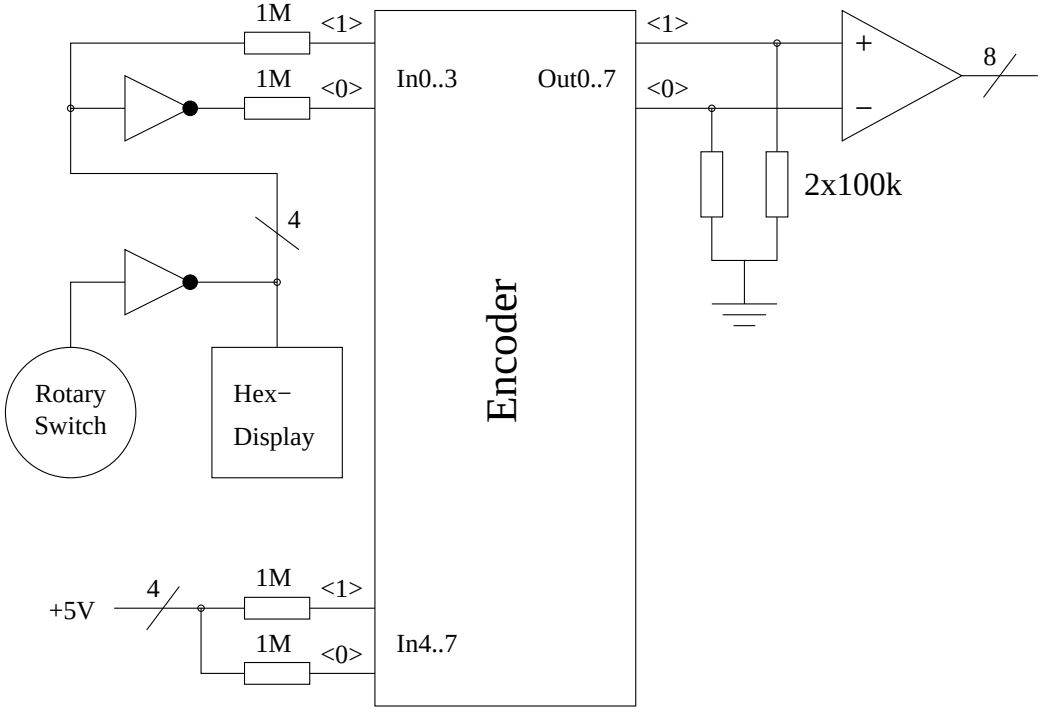

Figure 2: Partly schematic of the encoder

A hexadecimal rotary switch is provided to set the 4-bit dataword. The setting is visible on a 7-segment display.

The (8,4,4) Analog Hamming Decoder is operated as encoder. The four data bits are put straighforward to the chip: depending on the bit state a current is fed either to the `IN<0>` or the `IN<1>` pin. The parity inputs `IN4..IN7` are set to a neutral state with a balanced current pair. The decoder output delivers then not only the four data bits at `OUT0..OUT3` but also the parity bits at `OUT4..OUT7`.

The generated codeword is digitized by leading each current pair to a comparator.

Figure 2 does not show the full circuit: since all bits are treated equally only a single bit channel is drawn.

4 Channel

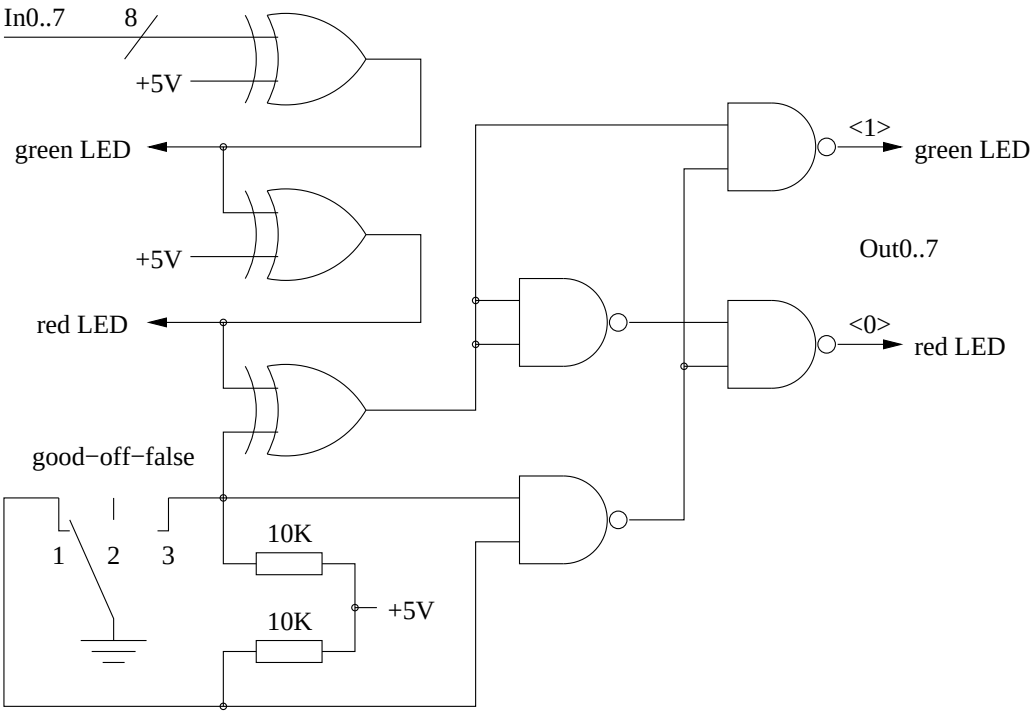

Figure 3: Bit manipulation on the channel

Each codeword bit can be manipulated with a rocker switch. At the first position the bit is left in it's original state. The second position passes a neutral bit probability to the decoder ignoring the bit state completely. The third position introduces a bit error by inverting the bit.

The advanced CMOS logic circuits 74AC00 and 74AC86 can source or sink 24mA. This is sufficient to drive the two colour LEDs.

5 Decoder

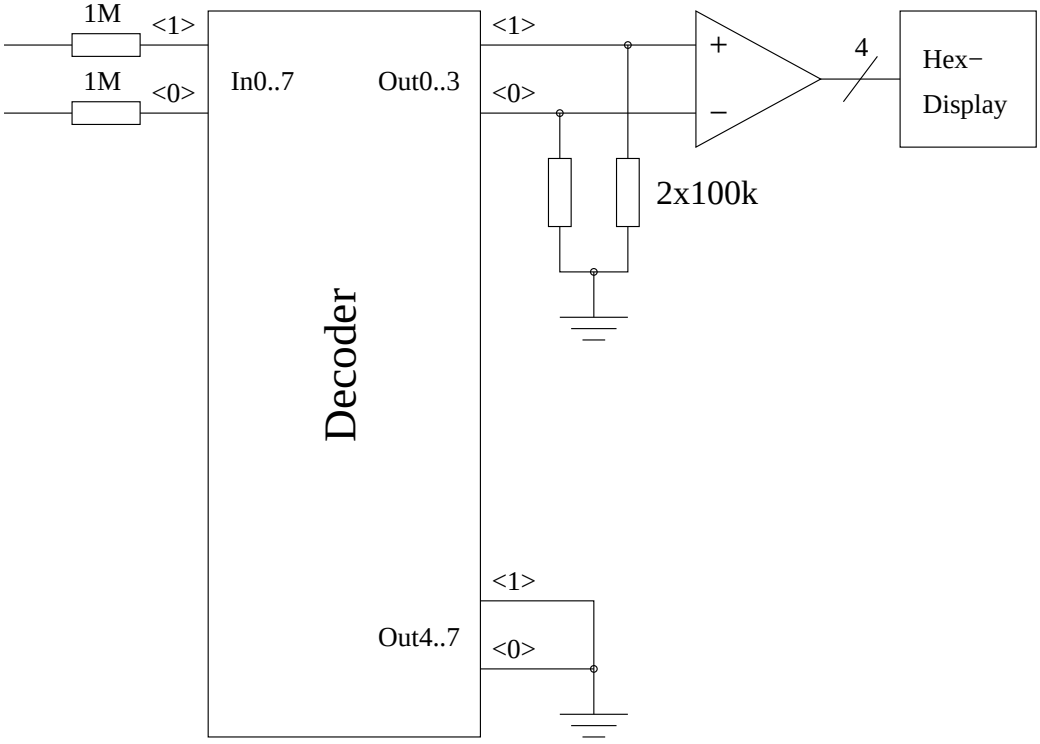

Figure 4: Schematic of the decoder

On this demonstation box the analog decoder sees only bit probabilities of 0, 0.5 and 1. In a real application the bits appearing at the decoder can have any value between 0 and 1.

The dataword at the decoder output is again digitized with comparators and shown on a hexadecimal display.

6 Examples

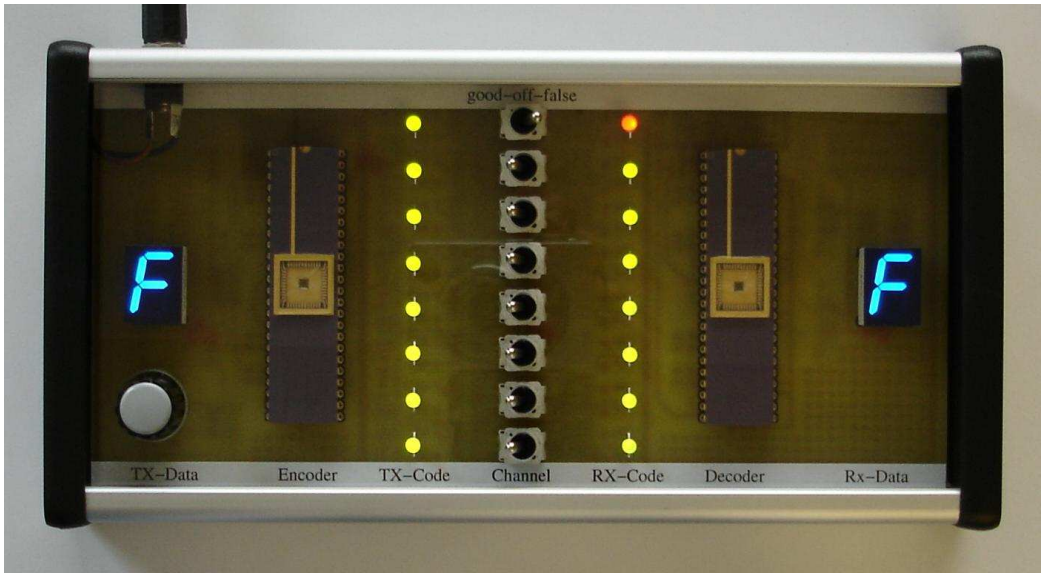

Figure 5: a single bit error is corrected

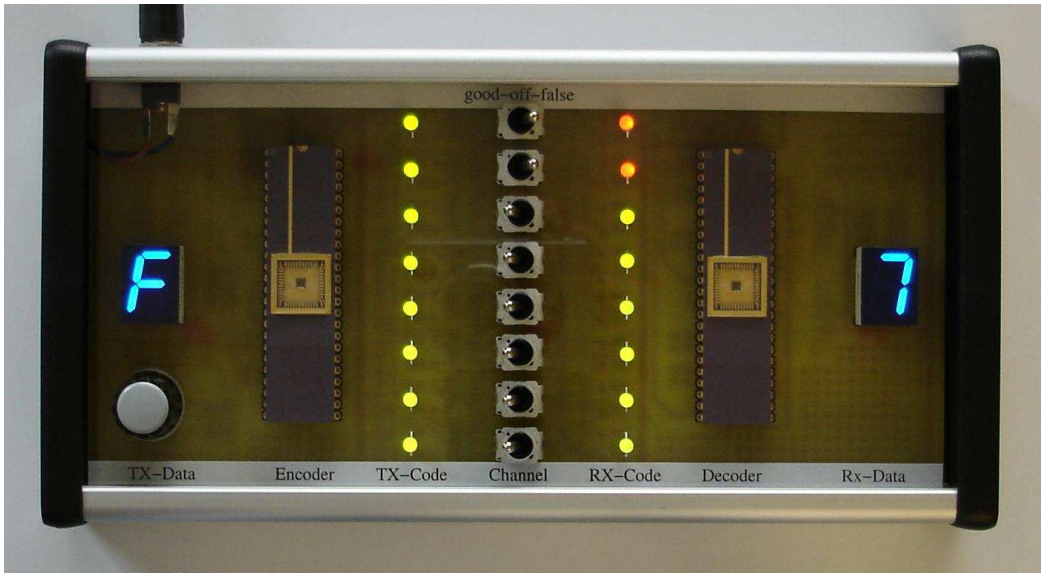

Figure 6: two bit errors cannot be corrected

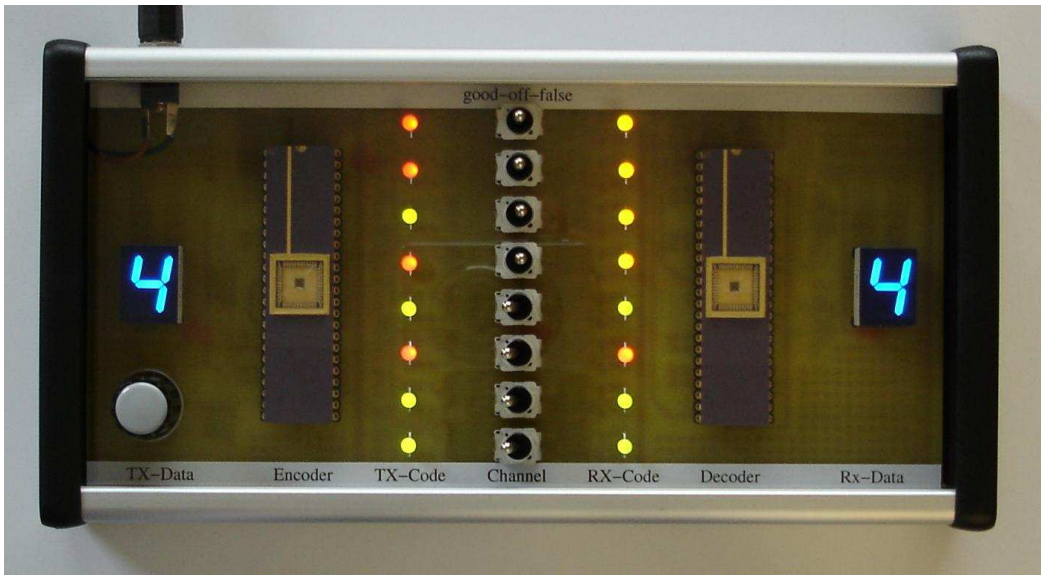

Figure 7: any four bits can be turned off

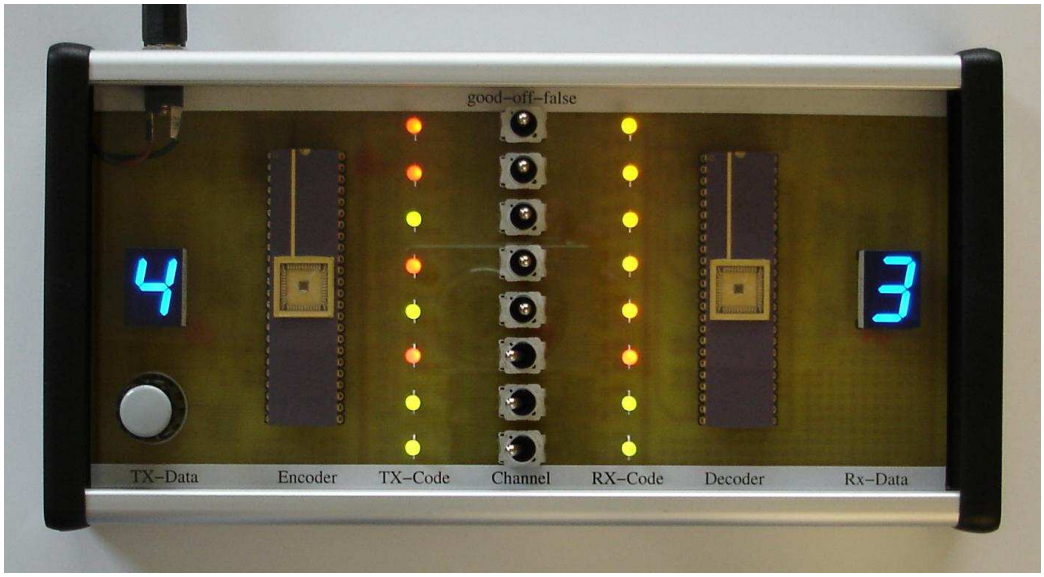

Figure 8: failure when five bits are turned off

7 Hexadecimal display

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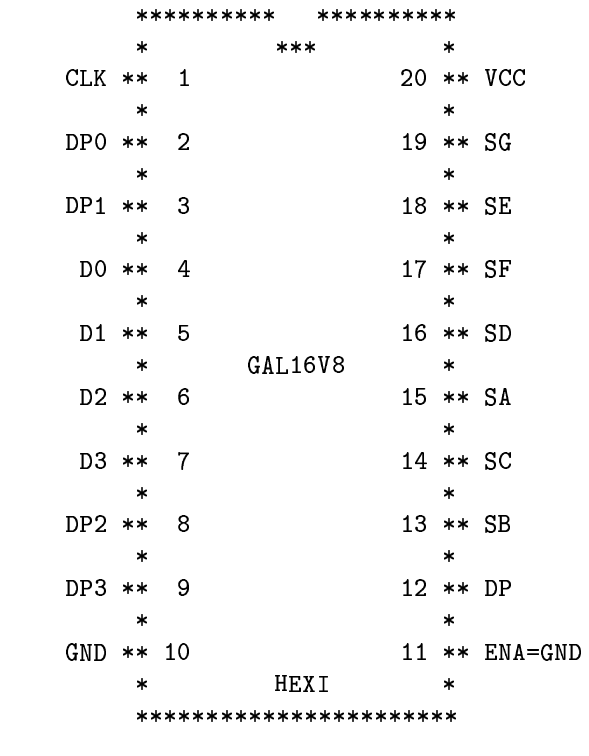
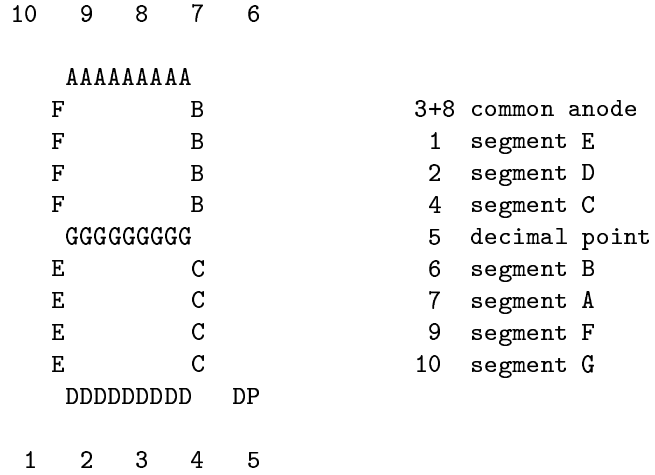
-------------------------------------------------------------------------
Hexadecimal 7-Segment Driver                GAL design specification
-------------------------------------------------------------------------
```





HEX	D3	D2	D1	D0	SA	SB	SC	SD	SE	SF	SG
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
A	1	0	1	0	1	1	1	0	1	1	1
B	1	0	1	1	0	0	1	1	1	1	1
C	1	1	0	0	1	0	0	1	1	1	0
D	1	1	0	1	0	1	1	1	1	0	1
E	1	1	1	0	1	0	0	1	1	1	1
F	1	1	1	1	1	0	0	0	1	1	1

```
Connections: GND = 0V, VCC = 5V, CLK = GND, ENA = GND.
             DP0, DP1, DP2, DP3 = GND if decimal point not used.
             Segment outputs with 220 Ohms to LED cathodes.


*IDENTIFICATION
    HEXI;

*TYPE
    GAL16V8;

*PINS
    DP0 = 2,
    DP1 = 3,
    D0 = 4,
    D1 = 5,
    D2 = 6,
    D3 = 7,
    DP2 = 8,
    DP3 = 9,
    DP = 12,
    SB = 13,
    SC = 14,
    SA = 15,
    SD = 16,
    SF = 17,
    SE = 18,
    SG = 19;
```

```
*BOOLEAN-EQUATIONS

    DP = /DP0 & /DP1 & /DP2 & /DP3;

    SA = /D3 & /D2 & /D1 &  D0
       + /D3 &  D2 & /D1 & /D0
       +  D3 & /D2 &  D1 &  D0
       +  D3 &  D2 & /D1 &  D0;

    SB = /D3 &  D2 & /D1 &  D0
       +        D2 &  D1 & /D0
       +  D3 &  D2 &       /D0
       +  D3 &        D1 &  D0;

    SC = /D3 & /D2 &  D1 & /D0
       +  D3 &  D2 &  D1
       +  D3 &  D2 &       /D0;

    SD = /D3 & /D2 & /D1 &  D0
       + /D3 &  D2 & /D1 & /D0
       +  D3 & /D2 &  D1 & /D0
       +        D2 &  D1 &  D0;

    SE = /D3 &              D0
       +       /D2 & /D1 &  D0
       + /D3 &  D2 & /D1;

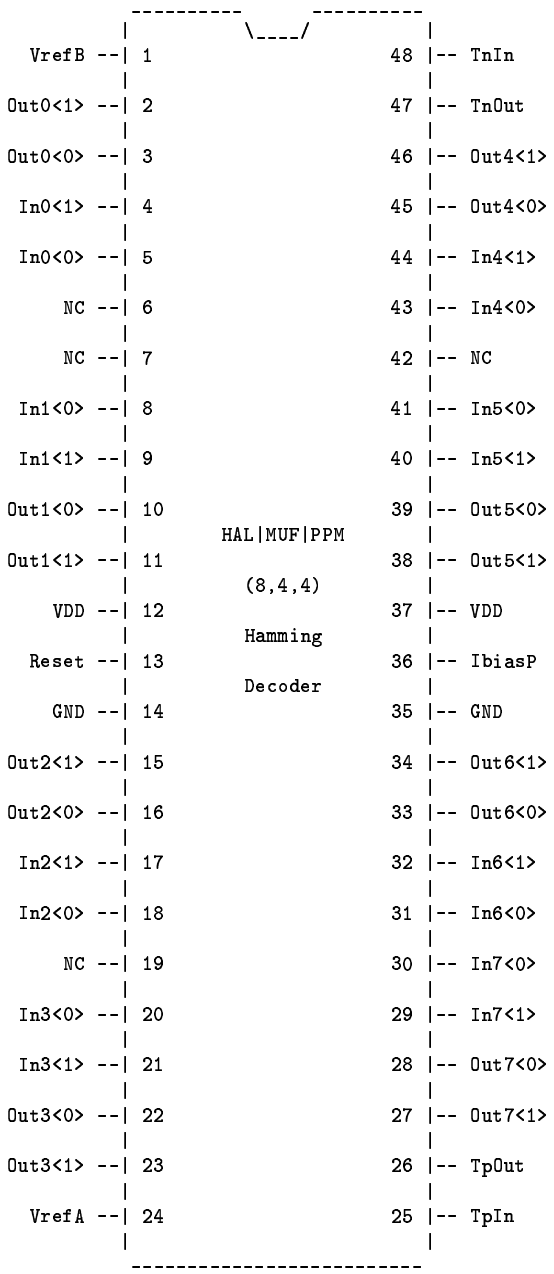
    SF = /D3 & /D2 &        D0
       + /D3 & /D2 &  D1
       + /D3 &        D1 &  D0
       +  D3 &  D2 & /D1 &  D0;

    SG = /D3 & /D2 & /D1
       + /D3 &  D2 &  D1 &  D0
       +  D3 &  D2 & /D1 & /D0;

*END
```

A GAL16V8 and a 7 segment LED display was used since there are currently no hexadecimal displays with a 4 bit parallel input available on the market (the TIL311 is no more available). Commercial 7 segment drivers support only BCD codes. The drawback of the display driver realized with a GAL is the rather high current consumption. A low power GAL draws a static current of about 70mA (maybe a controller like the PIC16F88 with a current consumption of 1μA would have been a better choice).

8 The (8,4,4) Analog Hamming Decoder



The chip is fabricated in an IBM 0.18μm CMOS process and mounted in a 0.3 Inches wide 48pin CERDIP.

Pin Description

`GND`	The two `GND` pins are connected to the common ground.
`VDD`	Both `VDD` pins are connected to a 1.8V supply.
`VrefA`	An Opamp is used to generate 0.45V for `REFA`.
`VrefB`	An Opamp is used to generate 1.35V for `REFB`.
`IbiasP`	Bias sets the working current for the analog decoder. The Pin is tied with a 1.0MΩ resistor to `VDD`.
`RESET`	When `RESET` is pulled up, internal reset transistors force the decoder to a neutral state. This pin should be connected to `GND` when not used.
`In0..In7`	Eight current pairs that feed the bit probabilities of the codeword to the decoder.
`OUT0..OUT7`	These eight pairs of output currents show the result of the decoding process.
`TnIn`	Gate of a single NMOS test transistor. The Source is connected to `GND`
`TnOut`	Drain of the single NMOS test transistor.
`TpIn`	Gate of a single PMOS test transistor. The Source is connected to `VDD`
`TpOut`	Drain of the single PMOS test transistor.