Swiss Federal Institute of Technology Zurich
Signal and Information Processing Laboratory

Analog Decoder Tester ADT02

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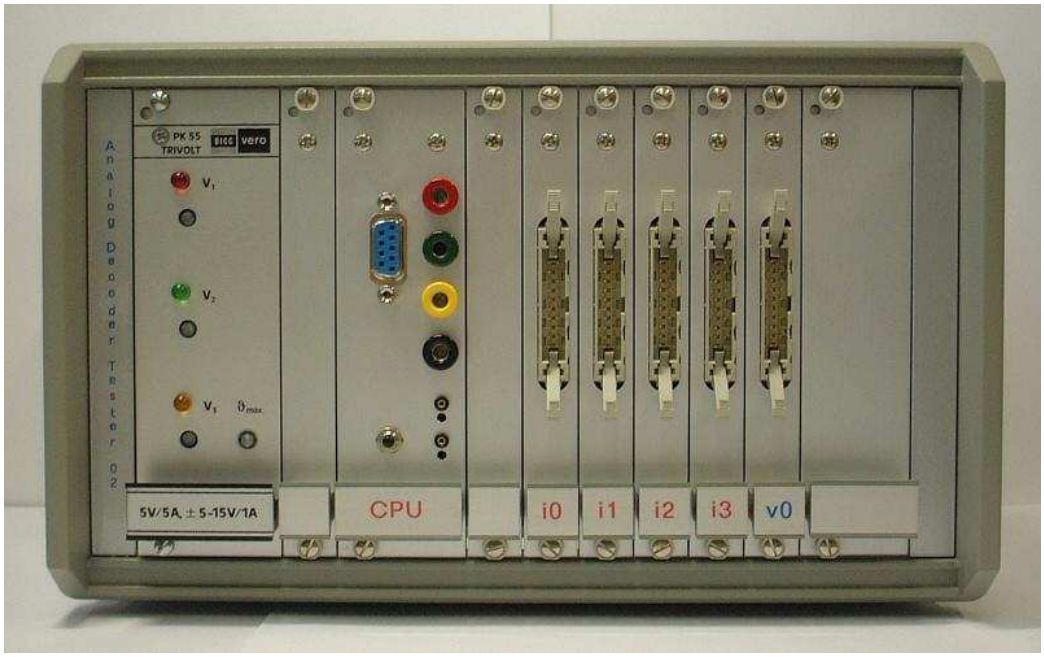
Contents

1 Overview

Figure 1: Front view



Purpose of the tester is to gain real-world results from analog decoders made of ESEQU and ESXOR Softgate chips for a comparison with theoretical and simulated characteristics.

The tester generates the necessary supply voltages and input currents to operate the decoder and measures the resulting output currents.

The ADT02 is made of modules that are arranged in an industry standard housing. There is a power supply, a CPU module and several analog I/O boards. A backplane provides internal electric interconnection and a serial interface is available for external communication.

2 Backplane

The backplane provides 10 slots with 96 pin DIN connectors in a spacing of 3/10 inches (15.24mm). A short description of bus signals is given below. Refer to Table 1 for the signal distribution on the bus.

D0..DA A 12 bit wide data bus allows reading and writing of ADCs and DACs in a single R/W-cycle. Although bus access to I/Os is asynchronous DACs and ADCs work synchronously while testing.

A0..A7 An 8 bit wide address bus gives enough address space for communication with several I/O devices.

LDAC A low pulse on LDAC updates all analog outputs according to their previously loaded registers.

CONVST A low pulse on CONVST samples all analog inputs and stores the results in the A/D converter registers.

RESET This active low signal is assigned to the D/A converter reset input and is currently not in use.

SHORT There is a CMOS switch between two adjacent current outputs for a fast reset of the tested analog decoder inputs. A *low* signal turns these switches on.

DR Direction of bus drivers. When DR is low, the CPU port is driven by the data bus. Since the I/O cards drive the bus directly from the A/D converters (without additional bus drivers) this signal is equal to RW.

RW High for write cycles, low for read cycles – from the CPU's point of view.

DS Data strobe. For write cycles this is a low pulse used to latch data on the rising edge. For read cycles data should be presented from the addressed I/O device while this signal is low.

Table 1: BUS Signals

A1	GND	B1	GND	C1	GND
A2	VCC	B2	VCC	C2	VCC
A3	GND	B3	GND	C3	GND
A4	DR	B4	GND	C4	RESET
A5	RW	B5	GND	C5	LDAC
A6	DS	B6	GND	C6	CONVST
A7		B7	GND	C7	SHORT
A8		B8	GND	C8	
A9		B9	GND	C9	
A10	A0	B10	GND	C10	A1
A11	A2	B11	GND	C11	A3
A12	A4	B12	GND	C12	A5
A13	A6	B13	GND	C13	A6
A14		B14	GND	C14	
A15		B15	GND	C15	
A16		B16	GND	C16	
A17		B17	GND	C17	
A18	D0	B18	GND	C18	D1
A19	D2	B19	GND	C19	D3
A20	D4	B20	GND	C20	D5
A21	D6	B21	GND	C21	D7
A22	D8	B22	GND	C22	D9
A23	D10	B23	GND	C23	D11
A24		B24	GND	C24	
A25		B25	GND	C25	
A26	+2.490V	B26	GND	C26	+2.490V
A27	+8.192V	B27	GND	C27	+8.192V
A28	-15V	B28	-15V	C28	-15V
A29	+15V	B29	+15V	C29	+15V
A30	GND	B30	GND	C30	GND
A31	VCC	B31	VCC	C31	VCC
A32	GND	B32	GND	C32	GND

3 Power Supply

A tripple voltage power supply is provided to operate the ADT02 directly from the 230V/50Hz power line. Maximum currents are 5A for the 5V output and 1A for the +15V and -15V outputs.

Table 2: Current Consumption

	5V	+15V	-15V
CPU (DSP56303 Board)	420mA	—	—
Single I/O Board	85mA	110mA	100mA
Cooler Fan	—	—	80mA
Total (with 5 I/O Boards)	845mA	550mA	580mA
Power	4.23W	8.25W	8.70W

A cooler fan on the rear side protects the device from overheating.

Figure 2: Rear view

4 CPU Module

4.1 Assembly

The CPU is built of a DSP56303 Evaluation Module that is attached to a prototyping board which provides the necessary glue logic to adapt the DSP's Host Interface Port to the backplane of the tester.

Table 3: DSP56303EVM Host Interface Port Connector

1	D0	2	D1
3	D2	4	D3
5	D4	6	GND
7	D5	8	D6
9	D7	10	RESET
11	D8	12	D9
13	D10	14	D13
15	D14	16	D12
17	+3.3V	18	D15
19	D11	20	GND

Common reference voltages that are used by all analog I/O boards are also generated on the CPU module.

The front panel has a 9 pin RS232 connector for uploading test programs and reading test results. A reset button terminates the current program and makes the tester ready to receive new program code. Above the reset button is a message-LED (a later modification, not yet visible on the photographs).

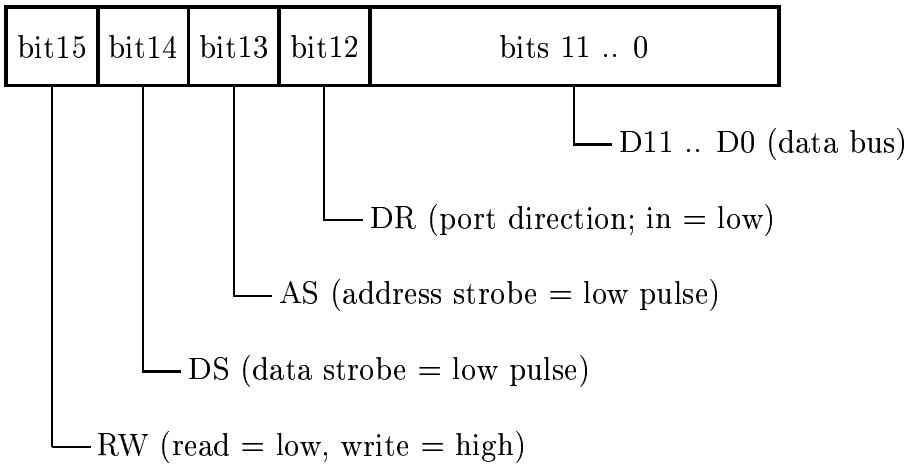
Supply voltages are available on 4mm sockets (GND = black, -15V = yellow, +15V = green, +5V = red).

Reference voltages (8.192V and 2.490V) are available on 1mm taps and adjustable with a small screwdriver.

4.2 Bus Access

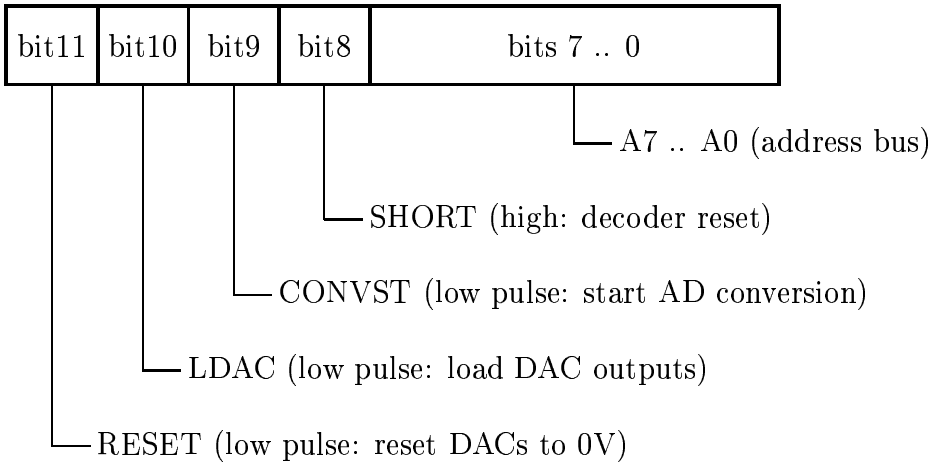
The Host Interface is used as a GPIO port and controlled through the Host Data Direction Register (HDDR X:$FFFFC8) and the Host Data Register (HDR X:$FFFFC9).

Figure 3: Host Data Register



Address and data busses are multiplexed at the Host Interface Port. AS latches data to the address/control bus:

Figure 4: Address/Control Bus



The bus is normally driven by the CPU module: RW (bit15) is set and all direction flags in the HDDR are set to output: HDDR = $FFFF.

Before RW is cleared for a read cycle, data lines *must* be set to inputs: HDDR = $F000. For a read operation RW is then taken low, so that it is free to be driven by an I/O device. Read cycles must be carefully programmed to avoid a bus conflict. Only the device with an address match may drive the bus. Data becomes valid at DS low.

A. Initialising the Hi08 Port

1. Enable GPIO in HPCR (set bit 0).
2. Set GPIO pins to out (HDDR = $FFFF).
3. Set RW, DS, AS, DR high (idle state of these signals!)

B. Setting the address/control bus

1. Take AS low, data bits to address/control pattern.
2. Take AS high.

C. Writing data to an I/O device

1. Set address/control (see *B*).
2. Take DS low, data bits as desired.
3. Take DS high.

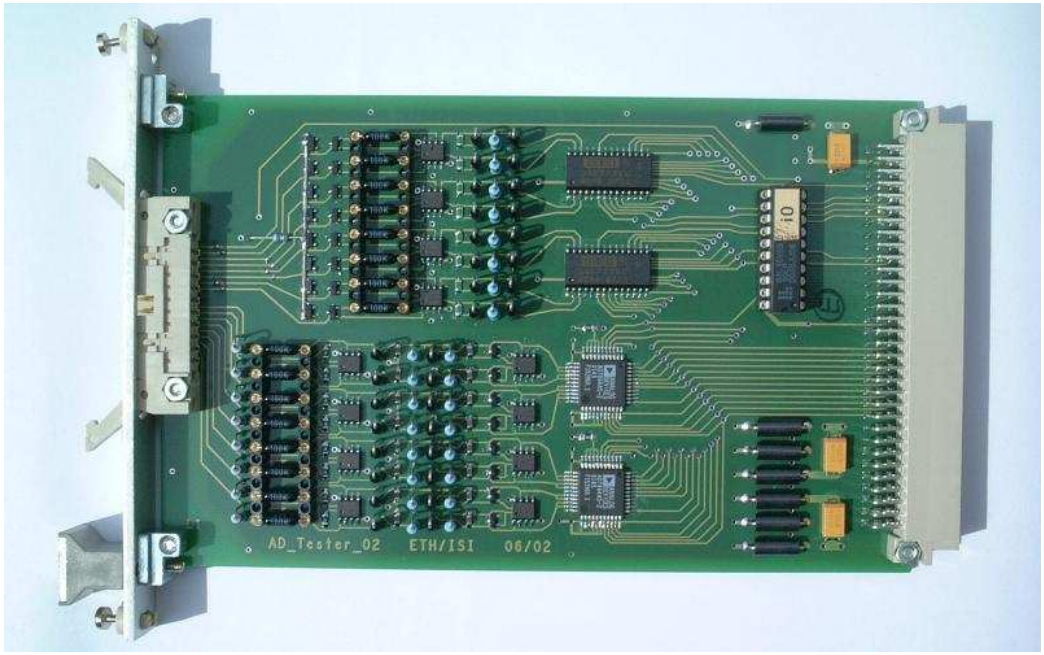
D. Reading from an I/O device

1. Set address/control (see *B*).
2. GPIO pins to input (HDDR = $F000).
3. Take DR and RW low.
4. Take DS low.
5. Read data (ignore bits 15..12).
6. Take DS high.
7. Take DR and RW high.
8. GPIO pins to output (HDDR = $FFFF).

5 Analog I/O Boards

5.1 Assembly

Figure 5: Analog I/O Board



Two DAC7725 (12-Bit Quad Voltage Output DACs) and two AD7864 (4-Channel 12-Bit ADCs) are placed on a four layer PCB. DAC voltage outputs are converted to current outputs and current inputs are adapted to the ADC voltage inputs. The eight inputs and outputs cover a current range from 0 to 2μA. This range may be changed by replacing socket mounted resistors.

An ADG711 Quad CMOS switch is provided to short pairs of current outputs to set inputs of a tested decoder to a neutral state.

Wire inductors, tantalum caps and some ceramic caps (on the bottom layer of the PCB) are used for decoupling the power supply and reference voltages.

A GAL16V8 incorporates address decoding and adaptation of control signals. The GAL16V8 source file *adt.gal* was modified for each analog I/O board to get an individual address.

Table 4: I/O Address Map

Address	Input or Output	Data	Physical Range
$00 .. $1F	current outputs 0..31	$FFF.. 0	0 .. 2047nA
$40 .. $5F	current inputs 0..31	0 .. $FFF	0 .. 2047nA
$80 .. $84	refa .. refd, vdd	0 .. $FFF	0 .. 8.194V

Preloaded outputs are updated after a low pulse on LDAC. Input conversion is started by a low pulse on CONVST and results are available after $7\mu s$. Note: Input registers are not addressable individually: The two least significant address bits are ignored while data is accessed by reading four times the same address.

The following extract from the GAL source file shows the pins and output equations for the first I/O module (i0):

```
% CS0, CS1 one to each DAC7725. %
% CS2, CS3 one to each AD7864.  %
% WR, RD to both AD7864.        %

*PINS

A7 = 2, A6 = 3, A5 = 4, A4 = 5,
A3 = 6, A2 = 7, DS = 8, RW = 9,
CS0 = 14, CS1 = 15, CS2 = 16, CS3 = 17,
RW_ = 12, DS_ = 13, RD  = 18, WR  = 19;

*BOOLEAN-EQUATIONS

/RW_ =  RW;
/DS_ =  DS;
/WR  =  RW * /DS;
/RD  = /RW * /DS;
/CS0 = /DS * /A7 * /A6 * /A5 * /A4 * /A3 * /A2;
/CS1 = /DS * /A7 * /A6 * /A5 * /A4 * /A3 *  A2;
/CS2 =       /A7 *  A6 * /A5 * /A4 * /A3 * /A2;
/CS3 =       /A7 *  A6 * /A5 * /A4 * /A3 *  A2;
```

Four analog I/O boards *i0* to *i3* are provided for current generation and measurement. A board can drive four decoder inputs and measure four outputs since an analog decoder needs *a pair* of currents for every input.

Table 5: Current module (i0 .. i3) Front Connector

20	out7	19	out6
18	out5	17	out4
16	out3	15	out2
14	out1	13	out0
12	GND	11	GND
10	in7	9	in6
8	in5	7	in4
6	in3	5	in2
4	in1	3	in0
2	GND	1	GND

One board *v0* is modified to deliver supply and reference voltages for the DUT (device under test) instead of currents. Fast OPA2132 amplifiers have been replaced by LM358 on this board since the former started oscillating caused by the load of bypass caps on the DUT.

Table 6: Supply Module (v1) Front Connector

20	refa	19	refa
18	refb	17	refb
16	refc	15	refc
14	refd	13	refd
12	GND	11	GND
10	—	9	—
8	vdd	7	vdd
6	—	5	—
4	—	3	—
2	GND	1	GND

5.2 Outputs

Figure 6: Output Stage

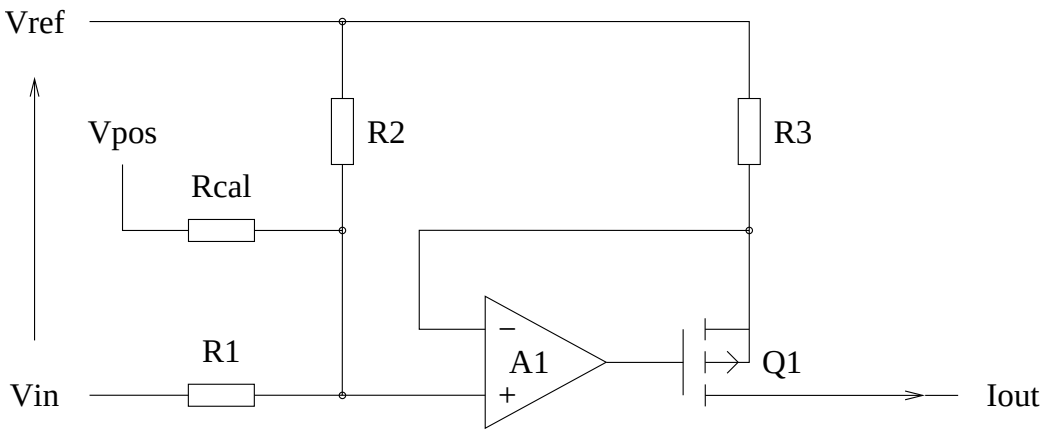


Figure 6 shows a single output stage. *Vref* is 8.192V. *Vin* comes from a DAC7725 output and ranges from *Vref* to 0V. *R1* and *R2* reduce the voltage by a factor of 40. The voltage over *R3* equals to that over *R2* and determines the output current. If *R3* is 100kΩ the output current is in the range from 0 to 2.048μA with a resolution of 12 bits (0.5nA per step).

Rcal is a high impedance resistor to *Vpos* (15V) and introduces an offset voltage to allow zero adjustment by software. *Rcal* has very little influence on the voltage divider formed by *R1* and *R2*.

5.3 Inputs

Figure 7: Input Stage

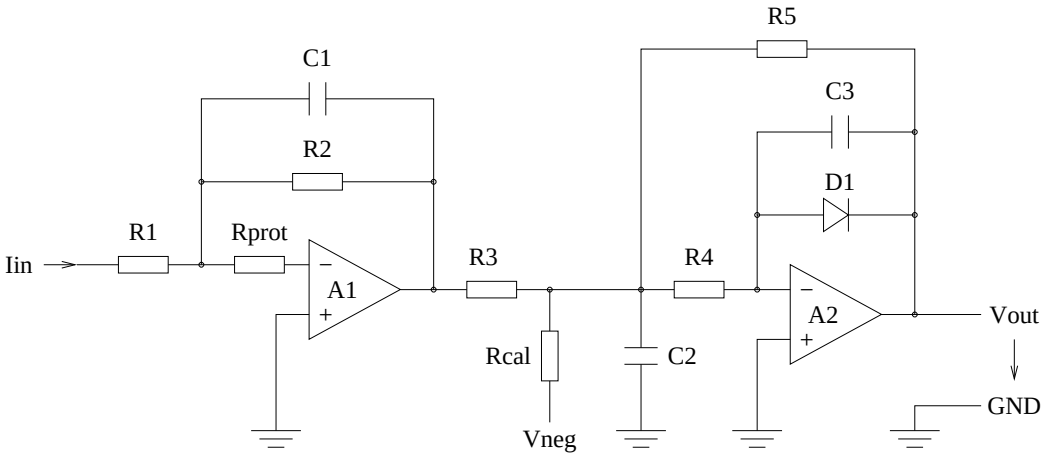


Figure 7 shows an input stage. If *R1* is a low impedance resistor, *A1* and *R2* form a current to voltage converter: $U_{out} = -I_{in} \cdot R2$.

A2 adjusts the output of *A1* to the analog-to-digital converter's input. The AD7864 converts voltages from 0 to 2.490V with a resolution of 12 bits. The gain of *A2* is determined by $-R5/R4$ and was chosen so that a current from 0 to 2.048μA with an *R2* of 100kΩ can be measured.

For voltage measurement *R1* may be replaced by a high impedance resistor; *A1* then works as an inverting voltage amplifier: $U_{out} = -Uin \cdot R2/R1$.

Rprot increases the overvoltage immunity of the input stage and has no influence on the circuit's function.

Rcal is a high impedance resistor to *Vneg* (-15V) and introduces an offset voltage to allow zero adjustment by software. *Rcal* has very little influence on the gain of A2.

D1 protects the AD7864: the datasheet allows a maximum negative voltage of -1V.

C1 rejects noise at the highly sensitive input. With *C2*, *C3* and *R4* added, *A2* forms a second order low pass filter.

6 Calibration

Although the OPA2132 operational amplifiers have low offset voltages it is still necessary to zero-adjust input and output stages. To keep the hardware as simple as possible, offset adjustment is done by software. Both input and output circuits have a resistor added that shifts the offset in one direction to allow offset correction by software, regardless whether the offset introduced by opamps was negative or positive.

Due to this offset adjustment much better channel matching is obtained. Full scale adjustment is not necessary because the critical resistors have high precision with a tolerance of 0.1% and all DACs and ADCs get the same reference voltages from the backplane.

Before starting with software calibration the supply voltages VDD = 5V, Vpos = 15V and Vneg = -15V as well as the reference voltages RefDAC = 8.192V and RefADC = 2.490V need to be checked. All these voltages are accessible and adjustable from the front of the tester.

Follow these instructions for software calibration of current inputs and outputs (modules i0 .. i3):

A. *Warm up*

   Turn the tester on for at least one hour before calibrating.

B. *Input calibration*

   Leave all inputs open and run the *calibi* program:

   ```
   dsplod -m calibi.lod
   ```

   The output of the program is an initialization string for the input calibration array *calibi*[ ]. Replace the old string in *tools.c* with this new string!

C. *Prepare output calibration program*

   For output calibration it is important that inputs are well adjusted. The *calibo* program must now be updated to get the input calibration data compiled in:

   ```
   g563c -o calibo.cld calibo.c
   cldlod calibo.cld >!  calibo.lod
   ```

D. Output calibration

Attach a shorting plug to the analog I/O connectors that connects outputs 0..7 to inputs 0..7. Run the *calibo* program:

```
dsplod -m calibo.lod
```

The output of the program is an initialization string for the output calibration array *calibo*[ ]. Replace the old string in *tools.c* with this new string! It is not necessary to short all I/O cards at the same time; calibrating may be done one by one: simply rerun the *calibo* program. Inputs that are left open should produce data in the range 198..201.

E. Update programs

Rebuild all test programs that include *tools.c*!

All calibration data should be positive integers in the range 0..80. If a value is negative the corresponding channel cannot be software-adjusted and the hardware must be checked. Occasionally an opamp with too much offset has to be replaced. A slightly negative value (say -1 or -2) may be corrected to 0.

7 Software

7.1 Code Development Tools

Free software development tools are available for Solaris – an assembler ASM56300 and the C cross compiler DSP563CCC.

All test programs have been written for the DSP563CCC compiler so far. Some low-level routines use in-line assembly supported by this compiler.

Free tools also include a simulator (sim56300) with a graphical user interface (gui56300), a syntax checker (lint563), a linker (dsplnk) and some small conversion tools. Hardware debugging tools (ads56300, gds56300) are available but need additional interface hardware (a command converter).

There are third-party tools for different platforms available, especially the *Tasking* compiler is said to be much superior to the free DSP563CCC.

7.2 Program Upload

First the environment variable DSPLOC must be set for the compiler to find include files. The PATH variable must include the directory for the dsp tools. e.g.:

```
setenv DSPLOC /disks/isibee29/strebel/56300
setenv PATH ${PATH}:/disks/isibee29/strebel/56300/dsp/bin
```

C sources can then be compiled to executable objectcode (.cld).

```
g563c -o test.cld test.c
```

This binary file may be converted to a loadable absolute code (.lod):

```
cldlod test.cld >!  test.lod
```

To upload this code to the DSP we have written the dsplod utility (use option -h to display a short help text):

```
dsplod test.lod
```

7.3 Interactive Measuring

For static measurements the program *measure* may be used. After uploading the program, communication through the serial interface is used to enter commands and display results:

```
dsplod -t measure.lod
```

At the beginning, a command summary is shown. An example session for a decoder that has to correct a single error is displayed below. It is set to 'output scaling' an the sum-current is 1000nA.

```
Commands:
---------
V vcc refa refb refc refd   set voltages    [mV]
i c0/c1 .. c14/c15          set currents    [nA]
o                           get currents    [nA]
S cs                        set sum current [nA]
I p0 .. p7                  set probs   [1/1000]
O                           get probs   [1/1000]
=                           display settings
ESC                         quit

>V 5000 0 1250 3750 3160
>S 1000
>I 900 100 100 100 100 100 100 100
>O 113 9 6 7 48 32 20 5
>o 108:848 10:1118 5:903 8:1115 51:1009 39:1166 22:1092 5:1098
>
```

7.4 Error Rate Measurement

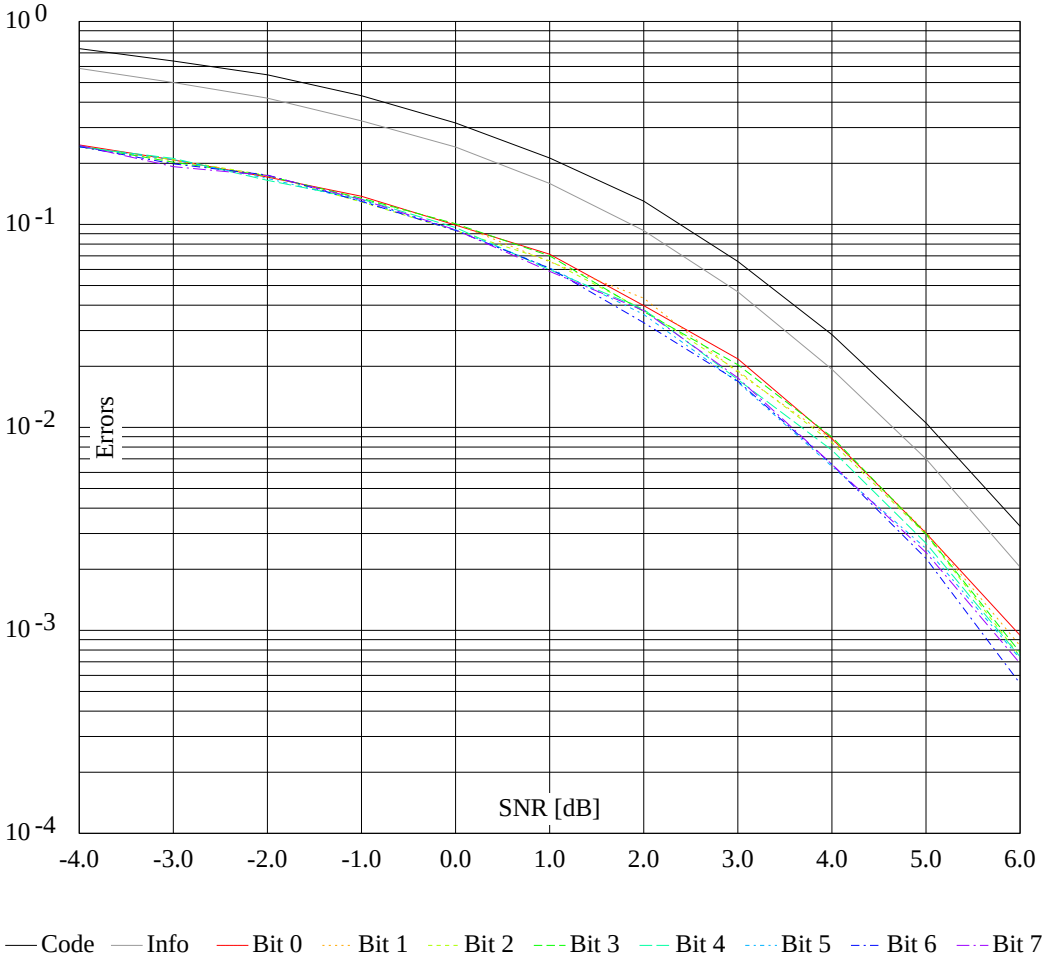
AWGN channel bit error rates are measured with the program *ber*:

```
dsplod -t ber.lod | tee -a ber.dat
```

Measured data is written to *stdout* and appended to a file. The tester shows its activity by blinking the message-LED. At completion, an ESC character is sent to leave the terminal mode of *dsplod*.

Parameters for the measurement are included in *ber.c* from the file *berpar.c* at compilation time. For graphical presentation of error rates, the data is saved in a matlab compatible format. Alternatively, the postscript file *ber.ps* can be used to interpret measured data for printing or displaying with ghostview.

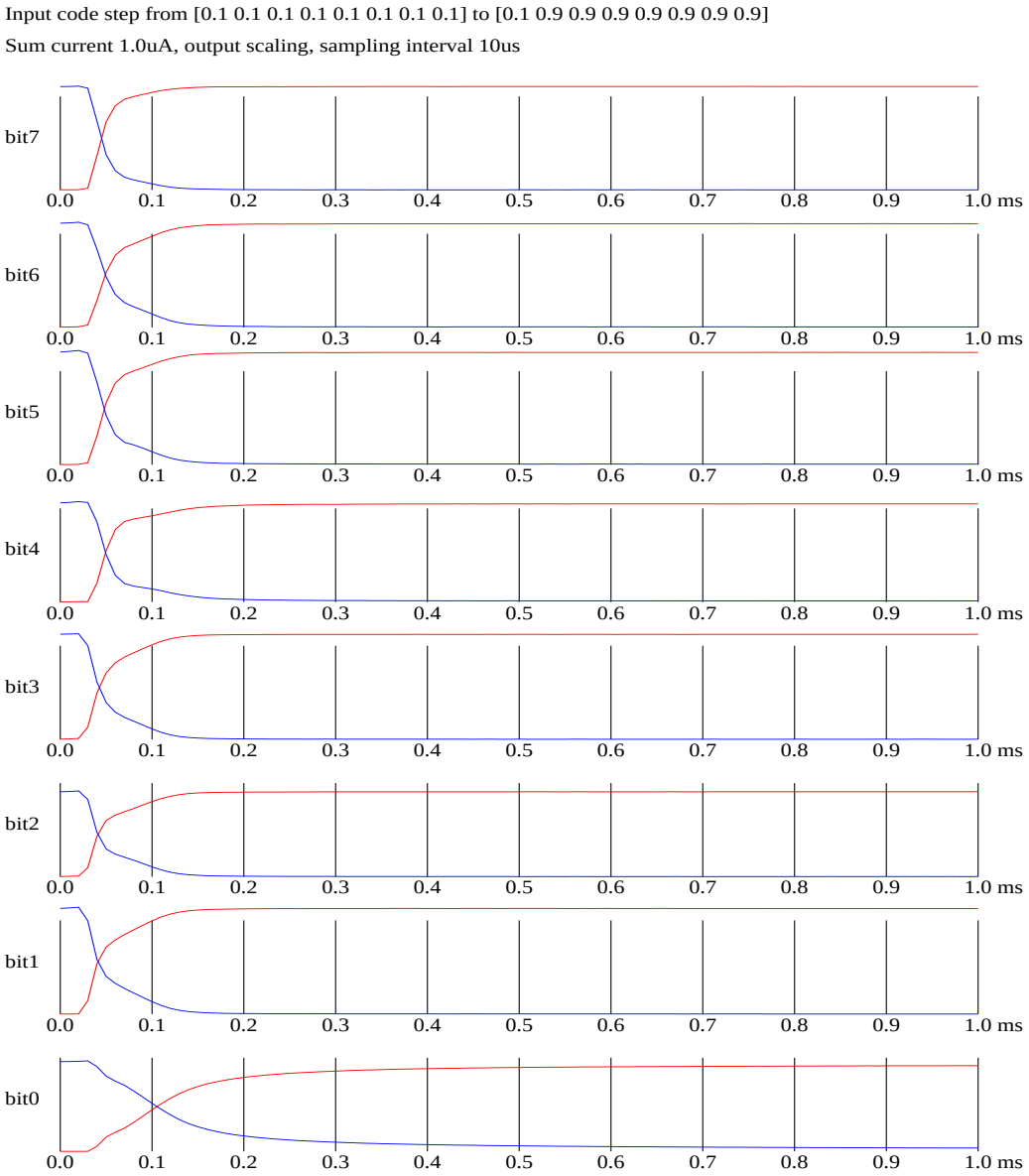
Figure 8: Measured AWGN Channel Error Rate Curve



7.5 Step Response Measurement

Another test program to observate settling characteristics of an analog decoder is *tim*. The following example shows a measurement with 101 samples in a distance of 10μs:

Figure 9: Measured Code Step Response



8 Additional Documentation

See the Motorola website (http://www.motorola.com) for DSP56300 tools and documentation.

`DSP56300FM.pdf`	DSP56300 Family Manual
`DSP56303UM.pdf`	DSP56303 User's Manual
`DSP56303DS.pdf`	DSP56303 Processor Data Sheet
`DSP56303EVMUM.pdf`	DSP56303 EVM User Manual
`DSPASMRM.pdf`	DSP Assembler Reference Manual
`DSP563CCC.pdf`	DSP56300 C Compiler User's Manual

Cadence Tools have been used to develop the analog I/O PCB. A schematic is stored under the project name *adt02* and split into the following sheets:

```
sheet 1      :  bus connections
sheet 2      :  front connections
sheet 3      :  chip selects, decoupling
sheet 4      :  inputs 0..3
sheet 5      :  inputs 4..7
sheet 6      :  outputs 0..3
sheet 7      :  outputs 4..7
```

PCB manufacturing was done from files listed below:

```
ger_top.art  :  top copper plane
ger_l2.art   :  intermediate copper plane 1
ger_l3.art   :  intermediate copper plane 1
ger_bot.art  :  bottom copper plane
ger_smt.art  :  top solder mask
ger_smb.art  :  bottom solder mask
ger_dd.art   :  dimensions and drilling
blendenliste :  gerber apperture list
drill.tap    :  excellon drill tape
```

The tester's performance depends highly on used analog components. Therefore the following datasheets are recommended for reading:

AD7864-2
: *Analog Devices*, AD7864, 4-Channel, Simultaneous Sampling, High Speed, 12-Bit ADC

DAC7725
: *Burr-Brown (Texas Instruments)*, 12-Bit Quad Voltage Output Digital-to-Analog Converter

OPA2132
: *Burr-Brown (Texas Instruments)*, OPA132, OPA2132, OPA4132, High Speed FET Input Operational Amplifiers

ADG711
: *Analog Devices*, ADG711, ADG712, ADG713, CMOS Low Voltage 4Ω Quad SPST Switches